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14. (Previously Added) A circuit arrangement as claimed in claim 7, characterized in that each of the inductive elements (12;22;32) comprises a plurality of turns.

REMARKS

This is responsive to the Action dated March 10th, 2003 in the above identified application. All claims stand rejected.

In the present response, claim 1 has been amended to clearly point out that the circuit arrangement is implemented on a metallization plate that is one of plural such plates, and which has the least ohmic resistance, as pointed out at pp.5-6 of the specification. Petrovic does not disclose this feature, which is critical for ensuring the highest possible Q filter. In fact, Petrovic appears largely or entirely directed to implementation of filters on PCBs, or "printed circuit boards", and thus, Petrovic includes no discussion of which metallization layer of a chip on which to implement anything. Accordingly, applicant respectfully requests withdrawal of the rejection of claim 1.

Claim 2 has been cancelled herein, rendering the prior rejection moot.

Claim 3 is believed patentable not only due to its dependency upon amended claim 1, but also due to its additional limitation of concentrically aligned inductors, as shown in figures 1 and 2 of the application. While Mizoguchi shows inductors arranged in a spiral, neither reference shows concentrically aligned inductors on an outer surface of an integrated circuit having the least ohmic resistance of all the surfaces. Accordingly, claim 3 is also believed patentable.

Claims 7-12 also stand rejected under 35 USC 102 over Petrovic. Claims 8-11 have been cancelled, and claim 7 is believed to be patentable due to its dependency upon claim 1 as well as its additional novel geometry of aligning at least three capacitors linearly in a row on the least ohmic resistive surface of a chip. Accordingly, reconsideration and allowance are respectfully requested.

Claims 1-14 are also rejected under 35 USC §103 as obvious over the combination of Petrovic and Mizoguchi. However, neither reference teaches to select one of plural layers of a chip that has the least ohmic resistance as the layer upon which to implement capacitive and inductive elements that are magnetically coupled to one another. Neither reference teaches concentrically aligned inductors with three or more linearly aligned capacitors (claims 3 and 7).

It is believed that the present amendment overcomes all of the rejections and places the case in condition for allowance. The applicant therefore respectfully requests reconsideration and allowance in view of the above remarks and amendments. The Examiner is authorized to deduct additional fees believed due from our Deposit Account No. 11-0223.

Respectfully submitted,

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Dated: June 10, 2003

Jeffrey I. Kaplan
(Reg. No. 34,356)

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal service as first class mail, in a postage prepaid envelope, addressed to Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on June 10, 2003.

Dated June 10, 2003 Signed Fern Pekarofski Print Name Fern Pekarofski

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Marked-up Version of Amended Claims 1, 3 and 7

1. (Currently Amended) A circuit arrangement for filtering and/or selecting single frequencies or frequency ranges of signals, said circuit arrangement (100) comprising at least two electric resonant circuits (10;20;30)

   - with at least an inductive element (12;22;32) and
   - at least a capacitive element (14;24;34),

   characterized in that the resonant circuits (10;20;30) are magnetically fixedly coupled to each other, and in that all the resonant circuits (10;20;30) of the circuit arrangement (100) are arranged on only one metallization plate (40) of an integrated circuit, having an essentially constant ohmic resistance, said metallization plate being one of plural, and being the one having the least ohmic resistance.

3. (Currently Amended) A circuit arrangement as claimed in claim 1, characterized in that the individual resonant circuits (10;20;30) are essentially arranged in a planar way on an outer surface area of the integrated circuit, and being arranged as concentrically aligned inductors.

7. (Currently Amended) A circuit arrangement as claimed in claim 1, characterized in that at least two inductive elements (12;22;32) which are substantially concentric and/or substantially parallel to each other. Said capacitive elements are arranged linearly with respect to each other and number at least three.